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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/739,839	12/20/2000	Yusuke Kawasaki	1080.1088/JDH	3883

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EXAMINER	
HENNING, MATTHEW T	
ART UNIT	**PAPER NUMBER**
2131	

DATE MAILED: 04/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/739,839	KAWASAKI ET AL.	
	Examiner	Art Unit	
	Matthew T. Henning	2131	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 December 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

This action is in response to the communication filed on 11/15/2004.

DETAILED ACTION

1. Claims 1-36 have been examined.

2. All objections and rejections not set forth below have been withdrawn.

Title

3. The title of the invention is acceptable.

Priority

4. The application has been filed under Title 35 U.S.C §119, claiming priority to Japanese application 2000212815, filed July 13, 2000.

5. The effective filing date for the subject matter defined in the pending claims in this application is July 13, 2000.

Information Disclosure Statement

6. The information disclosure statement (IDS) submitted on 01/31/2003 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the examiner is considering the information disclosure statement.

Drawings

7. The drawings filed on 12/20/2000 are acceptable for examination proceedings.

Specification

8. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: Claim 11 recites the limitation "ciphering and rewriting at least part of the information stored in said *internal* memory in a predetermined initialization operation".

Although there is support for ciphering and rewriting a portion of a flash memory in an initialization operation, the flash memory is an external memory as can be seen in Fig. 1 of the specification. Furthermore, there is no mention of ciphering and rewriting any part of the internal memory anywhere in the specification. Therefore, the specification is objected to for lacking antecedent basis for claimed subject matter. See the rejection of claims 11-17 and 19 under 35 USC 112 1st paragraph below.

Claim Objections

9. The applicant is reminded that a series of singular dependent claims is permissible in which a dependent claim refers to a preceding claim which, in turn, refers to another preceding claim.

A claim which depends from a dependent claim should not be separated by any claim which does not also depend from said dependent claim. It should be kept in mind that a dependent claim may refer to any preceding independent claim. In general, applicant's sequence will not be changed. See MPEP § 608.01(n).

Claim Rejections - 35 USC § 112

10. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> *The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.*

11. Claims 11-17, and 19 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the

relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claim 11 recites the limitation "ciphering and rewriting at least part of the information stored in said *internal* memory in a predetermined initialization operation". Although there is support for ciphering and rewriting a portion of a flash memory in an initialization operation, the flash memory is an external memory as can be seen in Fig. 1 of the specification. Furthermore, there is no mention of ciphering and rewriting any part of the internal memory anywhere in the specification. Therefore, claim 11 and its dependant claims 12-17 and 19 are rejected under 35 USC 112 1st paragraph for failing to comply with the written description requirement.

12. Claims 11-17 and 19 are rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for ciphering and rewriting at least a portion of an external memory (See Figures 1-2, 4, 15-19 and associated text of the specification), does not reasonably provide enablement for ciphering and rewriting at least a portion of an internal memory. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make the invention commensurate in scope with these claims. The ordinary person skilled in the art would not have been able to make and use the system as recited by claim 11 because the ordinary person would not know how a portion of the internal memory, which the specification discloses as being used to contain the operating system programs (See Specification page 18 Lines 17-20) could be encrypted and rewritten and still be able to operate. This is due to the fact that the specification does not disclose how the operating system can function if at least some of the operating system program instructions are overwritten with

encrypted versions of the instructions. Therefore, claim 11 and its dependant claims 12-17 and 19 are rejected under 35 USC 112 1st paragraph for failing to meet the enablement requirement.

13. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> *The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.*

14. Claims 14-17, and 29-35 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 14-15, 29 and 32-33 recite the limitation "said memory" or "the memory" but fail to distinguish which memory the limitation is referring to. The ordinary person skilled in the art would be unable to determine if the recitation was meant to refer to the "internal memory" or the "external memory" and therefore the ordinary person skilled in the art would not be able to determine the scope of the claim. Therefore, claims 14-15, 29, and 32-33 are rejected for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention. Claims 16-17, 30-31 and 34-35, are rejected by virtue of their dependency to one of the rejected claims above.

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> *(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.*

16. Claim 1 rejected under 35 U.S.C. 103(a) as being unpatentable over Taguchi et al. (U.S. Patent Number 5,915,025) hereinafter referred to as Taguchi, and further in view of Curran et al. (U.S. Patent Number 4,525,599) hereinafter referred to as Curran.

Taguchi disclosed an internal circuit (See Taguchi Fig. 31 Element 150) including a CPU executing programs (Element 151), at least one internal circuit having a predetermined function (Elements 152-157) and a bus line connecting said CPU to said internal device (See connection from 152 to 153 and 154), extending externally (See connection from 153 and 154 to 160) and transferring an address and data (See Col. 8 Lines 55-59), wherein said internal circuit includes at least one internal memory as an internal device (See Taguchi Fig. 31 Element 155 and Col. 13 Paragraphs 2-4 wherein it is disclosed that the key supply stores keys and retrieves keys upon request).

Taguchi further disclosed an external circuit (Elements 161-166) provided externally of an externally extending portion of said bus line (See all elements below 160) and including at least one external device having a predetermined function (Elements 161-166), wherein said external circuit includes at least one external memory as an external device (See Taguchi Fig, 31 Element 161 and Col. 8 Lines 33-36 wherein it was disclosed that the external storage was RAM (Random Access Memory).

Taguchi also disclosed that the internal circuit includes a ciphering section (Element 153) interposed at an entrance to an external side (See connection from 153 to 160) and ciphering the data on the bus line by ciphering patterns according to a plurality of regions divided from an address space allotted to entirety of said at least one external device (See Col. 8 Paragraph 5). However, Taguchi failed to disclose the ciphering of the address.

Curran teaches that software can be protected from illegal copying by encrypting the addresses of the data being accessed in order to provide a non-sequential ordering of the data in memory as well as encrypting the data stored therein (See Col. 1 Paragraph 5 – Col. 2 Paragraph 1 and Col. 3 Paragraph 3). It would have been obvious to the ordinary person skilled in the art at the time of invention to employ the teachings of Curran to the invention of Taguchi in order to encrypt the addresses as well as the data on the external bus. This would have been obvious because the ordinary person skilled in the art would have bee motivated to further protect the software and other data stored external from the data processor from illicit access.

17. Claims 2-3, 6-10, 18, 20-22, and 25-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Taguchi and Curran.

18. Claim 2 recites the ciphering patterns adopted by said ciphering section include one ciphering pattern in which neither the address nor data is ciphered (See Taguchi Col. 18 Paragraph 2 wherein only part of the data is encrypted).

19. Claim 3 recites that the external circuit includes a plurality of external devices (See Taguchi Fig. 31 Elements 161-166), and said ciphering section performs ciphering using ciphering patterns according to said plurality of external devices, respectively (See Taguchi Fig. 15).

20. Claim 6 recites the ciphering pattern determination means for recognizing a constitution of said external circuit and determining a ciphering pattern of said ciphering section according to the constitution of said external circuit (See Taguchi Col. 9 Paragraph 5 – Col. 10 Paragraph 1).

21. Claim 7 recites that the said ciphering section ciphers the address and the data on said bus line by ciphering patterns according to the plurality of regions divided from the address space

allotted to the entirety of said no less than one external device and according to application programs executed by said CPU (See Fig. 15 and Col. 8 Lines 55-63).

22. Claim 8 recites a deciphering section connected to the externally extending portion of said bus line, and returning the ciphered address and the data on the bus line to an address and data which are not ciphered (See Taguchi Fig. 31 Element 154 and Col. 10 Lines 25-27).

23. Claim 9 recites ciphering pattern change means for changing a ciphering pattern whenever a predetermined initialization operation is carried out for one of the plurality of regions divided from the address space allotted to the entirety of said at least one external device (See Taguchi Fig. 11, Fig. 13, and Fig. 15).

24. Claim 10 recites that the ciphering section adopts a ciphering pattern in which ciphered data is changed according to the address, for one of the plurality of regions divided from the address space allotted to the entirety of said at least one external device, to thereby cipher the data (See Taguchi Fig. 11, Fig. 13, and Fig. 15).

25. Claim 18 recites that the internal circuit holds a ciphering pattern adopted by said ciphering section (See Taguchi Fig. 31 Element 155), the processing apparatus further comprises a tamper detection section detecting tamper, and ciphering pattern destruction means for destroying the ciphering pattern held in said internal circuit in response to tamper detection made by said tamper detection section (See Col. 9 Paragraph 2).

26. Claim 20 is rejected for the same reasons as claim 1 above.

27. Claim 21 is rejected for the same reasons as claim 2 above.

28. Claim 22 is rejected for the same reasons as claim 3 above.

29. Claim 25 is rejected for the same reasons as claim 6 above.

30. Claim 26 is rejected for the same reasons as claim 7 above.

31. Claim 27 is rejected for the same reasons as claim 9 above.

32. Claim 28 is rejected for the same reasons as claim 10 above.

33. Claim 29 recites an internal circuit including a CPU executing programs, at least one internal device having a predetermined function, wherein at least one internal device is an internal memory (See Taguchi Fig. 31 and Col. 13 Paragraphs 2-4 wherein it is disclosed that the key supply stores keys and retrieves keys upon request); and a bus line connecting said CPU to said internal device, extending externally (See Taguchi Fig 31 and Claim 1 rejection), an external circuit including at least one external memory as an external device storing information provided externally of the externally extending portion of said bus line (See Taguchi Fig. 31 Elements 161 and 166) and transferring an address and data (See Taguchi Fig 31 and Claim 1 rejection); wherein said internal circuit has information rewrite means for ciphering and rewriting at least part of the information stored in said memory in a predetermined initial operation (See Taguchi Fig. 13).

34. Claim 30 recites that the predetermined initial operation is an initialization operation when the power is first turned on. Taguchi disclosed checking for expiration of keys and updating the keys and re-ciphering accordingly (See Taguchi Fig. 12 and Fig 13). It was inherent that in order for proper key management, the expiration times were checked constantly, or else the keys would have expired unknowingly. Therefore, it was also inherent that the expiration times were checked upon power up, which constitutes an initialization procedure.

35. Claim 31 recites the information rewrite means generates a random number, and performs ciphering by adopting a ciphering pattern using the generated random number (See Taguchi Col. 14 Lines 4-6).

36. Regarding claims 32-35, see Taguchi Col. 21 Paragraphs 5-6.

37. Claim 36 is rejected for the same reasons as claims 1 and 7 above.

38. Claims 4 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Taguchi and Curran as applied to claims 1 and 20 respectively above, and further in view of IBM (IBM Technical Disclosure Bulletin 19800601).

The combination of Taguchi and Curran disclosed the use of random number in generating keys (See Taguchi Col. 14 Lines 4-6), but the combination of Taguchi and Curran failed to disclose any information regarding times when the external bus was not being used.

IBM teaches that memory can be tested by generating random addresses, storing random data to the random addresses, and then checking that the generated data and the stored data are consistent.

It would have been obvious to the ordinary person skilled in the art at the time of invention to employ the teachings of IBM in the combination of Taguchi and Curran in order to test the memory when the external bus was not in use. This would have been obvious because the ordinary person skilled in the art would have been motivated to ensure that the external memory was working properly, thus ensuring data integrity.

39. Claims 5 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Taguchi and Curran as applied to claims 1 and 20 respectively above, and further in view of Milhaupt et al. (U.S. Patent Number 5,706,445) hereinafter referred to as Milhaupt.

The combination of Taguchi and Curran disclosed the use of a processor and a separate encryption circuit (See Taguchi Fig. 31), but failed to disclose using separate clocks with the encryption clock being set at a higher frequency than the processor clock. However, Taguchi and Curran did disclose that when encrypted software was input to the system at the CD-ROM drive (See Taguchi Fig. 31) the decryption means had to decrypt the software and then the encryption means had to encrypt the software and store the software in memory before the processor could access the software (See Taguchi Col. 10 Paragraph 1).

Milhaupt teaches that reducing the clock rate to the processor during times when the processor is not being used can dramatically reduce the power consumed by a processor.

It would have been obvious to the ordinary person skilled in the art to employ the teachings of Milhaupt in the combination of Taguchi and Curran in order to modulate the clock to the processor. This would have been obvious because the ordinary person skilled in the art would have been motivated to reduce the power consumed by the data processor while the processor was idle and waiting for the software to be re-encrypted and stored in memory.

40. Claims 11-17 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Taguchi and Curran as applied to claim 29 above, and further in view of Schneier.

41. Regarding claim 11, the combination of Taguchi and Curran disclosed a processing apparatus comprising: an internal circuit including a CPU executing programs, at least one internal device having a predetermined function, and a bus line connecting said CPU to said internal device, extending externally and transferring an address and data, wherein said internal circuit includes at least one internal memory as an internal device; and an external circuit

provided externally of the externally extending portion of said bus line, and storing information, wherein said external circuit includes at least one external memory as an external device, wherein said internal circuit has information rewrite means for ciphering and rewriting at least part of the information stored in said memory in a predetermined initialization operation (See the rejection of claim 29 above), but failed to disclose that the ciphered and rewritten portion was from the internal memory. However, the combination of Taguchi and Curran did disclose that the internal memory was a key storage (See Taguchi Col. 13 Paragraphs 2-4)

Schneier teaches that a key should never be un-enciphered outside its encryption device and that stored keys can be stored in encrypted form (See Schneier Page 18 Lines 20-28). It would have been obvious to the ordinary person skilled in the art at the time of invention to employ the teachings of Schneier in the key storage of Taguchi and Curran by encrypting the keys in the memory. This would have been obvious because the ordinary person skilled in the art would have been motivated to protect the keys that were stored outside of the encryption device.

42. Claims 12-17 are rejected for the same reasons as claims 30-34 as applied to claim 11 above.

43. Claim 19 is rejected for the same reasons as claim 18 as applied to claim 11 above.

Response to Arguments

44. Applicants' arguments filed 11/15/2004 have been fully considered but they are not persuasive. Applicants argue primarily that:

i. Taguchi fails to disclose "an external circuit".

ii. Taguchi Fig. 31 Element 150 does not include "an internal memory".

iii. The combination of Taguchi and Curran failed to disclose an internal circuit with an internal memory and an external circuit with an external memory.

iv. Taguchi and Curran fail to disclose the advantage of preventing illicit accesses to an internal memory via an add-on external device as in the claimed invention.

45. In response to applicants' argument iv., that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., preventing illicit accesses to an internal memory via an add-on external device) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Therefore, the examiner does not find the argument persuasive and will not address this argument further.

46. In response to the applicants' argument i. that Taguchi fails to disclose "an external circuit", the examiner does not find the argument persuasive. Taguchi clearly depicts a protective enclosure 150 (See Taguchi Col 25 Paragraph 9) containing circuitry internal to the enclosure (Elements 151-157), and further disclosed circuitry external to the enclosure (Elements 161-166) connected to the internal circuitry via a bus (Element 160). Therefore, the examiner does not find the applicants' argument persuasive.

47. In response to the applicants' argument ii. that Taguchi Fig. 31 Element 150 does not include "an internal memory", the examiner does not find the argument persuasive. Taguchi clearly depicted a key supply means 155 in Fig. 31. Taguchi also disclosed that the key supply stored and retrieved keys (See Taguchi Col. 13 Paragraphs 2-4). Microsoft Press Computer

Dictionary Third Edition defines "memory" as "a device where information can be stored and retrieved." Therefore, Taguchi did in fact disclose an internal memory. As such, the examiner does not find the argument persuasive.

48. In response to applicants' argument iii. that the combination of Taguchi and Curran failed to disclose an internal circuit with an internal memory and an external circuit with an external memory, the examiner does not find the argument persuasive. The combination of Taguchi and Curran clearly depicted an internal circuit with in internal memory (See Taguchi Fig. 31 Elements 150 and 155 and previous paragraph) and an external circuit (See response to argument i.) with an external memory (See Taguchi Fig. 31 Element 161 and Col. 8 Lines 33-36 wherein Taguchi disclosed that the storage was Random Access Memory). Therefore, the examiner does not find the applicants' argument persuasive.

49. Because the applicants' arguments have not been found persuasive, the examiner has maintained the rejections of claims 1-10, 18, and 20-35. The examiner has also maintained the rejections of claims 11-17, 19, and 36 due to the same reasoning as presented above applied to the new grounds of rejection presented above.

Remarks

50. The examiner has not considered the prior art references AG, AH, and AL from the IDS submitted on 1/31/2003, because they do not comply with 37 CFR 1.98(a)(3) because no English translation was provided for the references and no explanation of the relevance of the references was provided. As such, the examiner was not able to consider the references.

Conclusion

51. Claims 1-36 have been rejected.

52. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Best (U.S. Patent Number 4,168,396) disclosed a microprocessor for executing encrypted software, involving the combination of the data with its address.

b. Best (U.S. Patent Number 4,278,837) disclosed a microprocessor for executing encrypted programs in which the addresses for the data were scrambled prior to storage.

c. Westheimer et al. (U.S. Patent Number 4,573,119) disclosed a method of software protection involving encrypting both the data and address of the software.

d. Grider et al. (U.S. Patent Number 5,515,540) disclosed a method of data security involving encrypting the data and address as well as employing a tamper protection circuit.

e. Little et al. (U.S. Patent Number 6,272,637) disclosed a method of data security involving encrypting the data and address as well as employing a power monitoring circuit.

53. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

54. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

55. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew T. Henning whose telephone number is (571) 272-3790. The examiner can normally be reached on M-F 8-4.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ayaz Sheikh can be reached on (571) 272-3795. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Art Unit 2131
4/21/2005

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